

SOURCE: (C) IBM CORP 1993

P.D. 04 70

p. 1-2

(2)

AN : NN70041899

PUB : IBM Technical Disclosure Bulletin, April 1970, US

VOL : 12

NR : 11

PG : 1899 - 1900

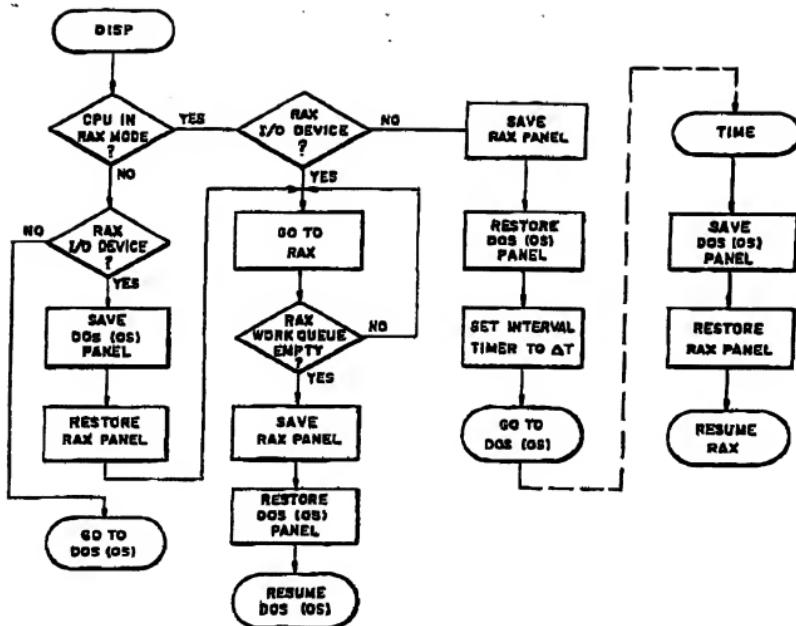
TI : Dual System Operation. April 1970.

TXT : 2p. This method allows two operating systems, i.e., IBM System/360 Remote Access Computing System (RAX) and IBM System/360 Disk Operating System (DOS) or IBM System/360 Operating System (OS), to operate concurrently sharing a standard System/360 processor and the core storage. The two systems have separate work loads and operate independently of each other as two autonomous operating systems. A software interface allows RAX, a time sharing terminal operating system, to share a central processing unit CPU with DOS or OS permitting a wider range of concurrent CPU usage and improving its throughput.

- In this mode of operation, the core storage is logically partitioned into two areas, and DOS or OS operates in the low-core area while RAX operates in the high-core area. The logical partitioning is opaque to both operating systems, and is transparent only to the Dispatcher routine. The Dispatcher saves and restores the status of the system, i.e., the Program Status Word Area, locations 0...127, and the general and floating point registers, each time it transfers control of the CPU from one system to another across the logical partitioning. The Dispatcher intercepts all I/O interrupts at all times. The low-core area is the CPU's home operating area. Control of the CPU is transferred to the RAX domain only on demand, i.e., an I/O interrupt from a device assigned to RAX. Control of the CPU is returned to the low-core area at the point of the I/O interruption at the end of the RAX operations.

- In the event of an I/O interrupt from a device assigned to DOS or OS while the CPU is operating in the RAX domain, control of the CPU is transferred to DOS or OS I/O interrupt processor with the timer set to a fraction of the time quantum of the RAX time-slice. Control of the CPU is returned to RAX either at the end of this time interval or on an I/O interrupt from a RAX device, whichever occurs first.

Dispatcher : CPU-Verwaltung



DISP AN ENTRY POINT IN THE DISPATCHER ROUTINE, ENTERED UPON AN I/O INTERRUPT. THE INSTRUCTION ADDRESS OF THE I/O NEW PSW POINTS TO DISP AT ALL TIMES.

PANEL THE STATUS OF THE SYSTEM; i.e., THE PROGRAM STATUS WORD AREA (CORE LOCATION 0-127) AND THE GENERAL AND FLOATING POINT REGISTERS.

ΔT A FRACTION OF THE TIME QUANTUM OF THE RAX TIME-SLICE.

TIME A SECONDARY ENTRY POINT IN THE DISPATCHER ROUTINE, ENTERED UPON THE EXTERNAL INTERRUPT AT THE END OF ΔT.